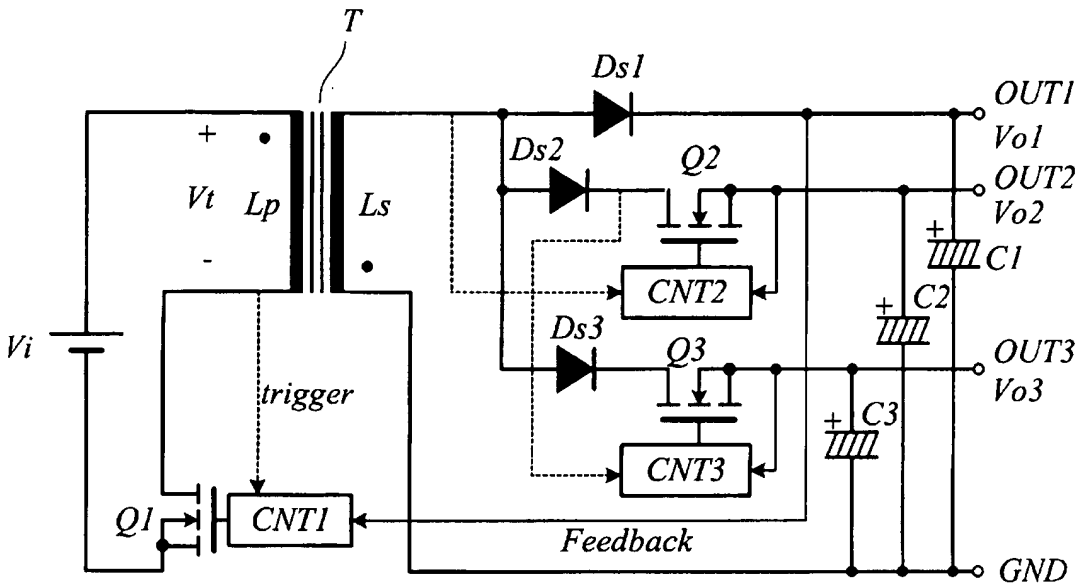
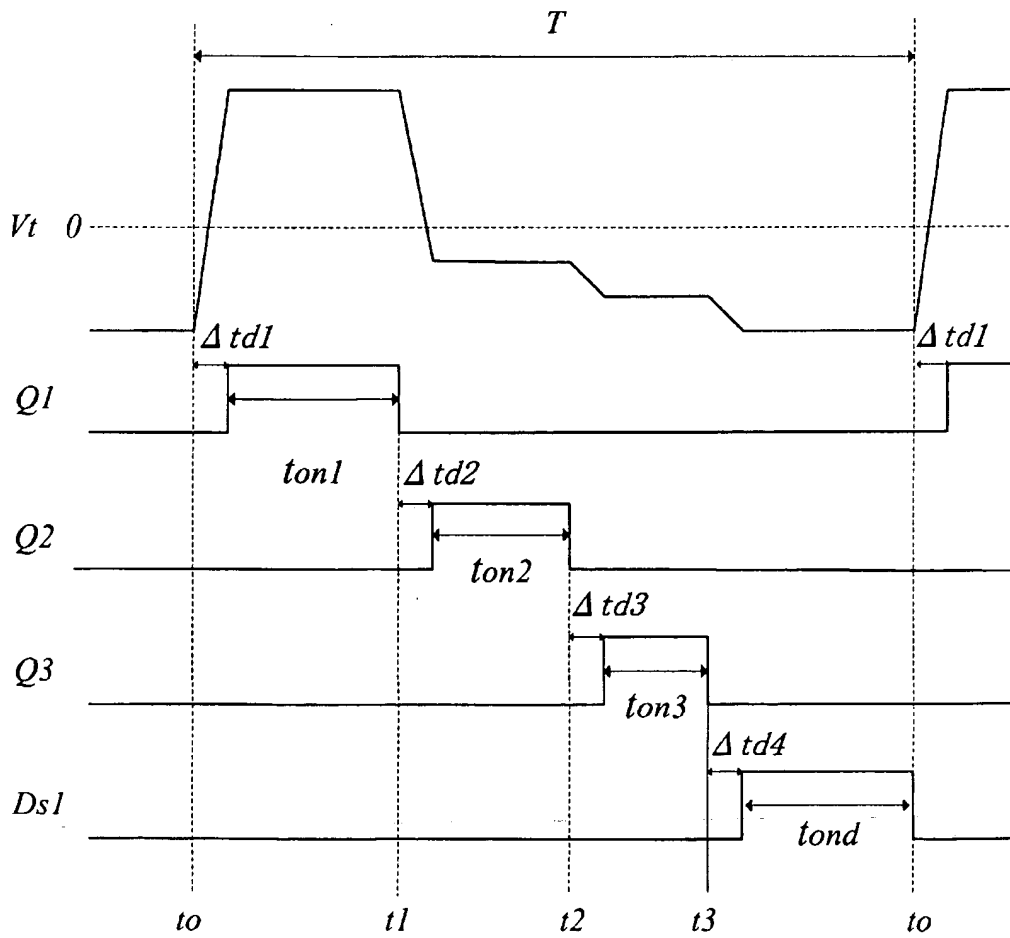


**FIG. 1A**



**FIG. 1B**



**FIG. 2A**

The circuit diagram shows a power converter. A DC voltage source  $V_i$  is connected to the gates of two MOSFETs,  $Q1$  and  $Q2$ . The source of  $Q1$  is grounded, and its drain is connected to the primary winding of a transformer. The source of  $Q2$  is connected to the secondary winding of the transformer, and its gate is connected to a feedback loop. The primary winding has inductance  $L_p$  and voltage  $V_t$  across it. The secondary winding has inductance  $L_s$  and is connected to a diode  $D_s$  in series with a load capacitor  $C_o$  and output voltage  $V_o$ . A feedback loop labeled "Feedback" connects the output  $V_o$  to the gate of  $Q1$ . Another feedback loop labeled "Feedback" connects the output  $V_o$  to the gate of  $Q2$ . A trigger signal is connected to the gates of both  $Q1$  and  $Q2$ . A capacitor  $C_r$  and a voltage  $V_c$  are connected to the gate of  $Q2$ . A transformer core is indicated by two vertical lines with dots on the windings. The transformer is labeled  $T$ .

The diagram shows three waveforms over time. The top waveform,  $V_t$ , is a reference voltage with a period  $T$ . The middle waveform,  $Q_1$ , is a pulse-width modulated signal with a pulse width  $ton1$  and a dead time  $\Delta t1$  after the pulse. The bottom waveform,  $Q_2$ , is a pulse-width modulated signal with a pulse width  $ton2$  and a dead time  $\Delta t2$  after the pulse. The period  $T$  is marked between two consecutive  $Q_1$  pulses. The time intervals  $ton1$  and  $ton2$  are marked with horizontal arrows. The dead times  $\Delta t1$  and  $\Delta t2$  are marked with vertical arrows. The time axis is marked with  $t_0$  and  $t_1$ .

FIG. 3A

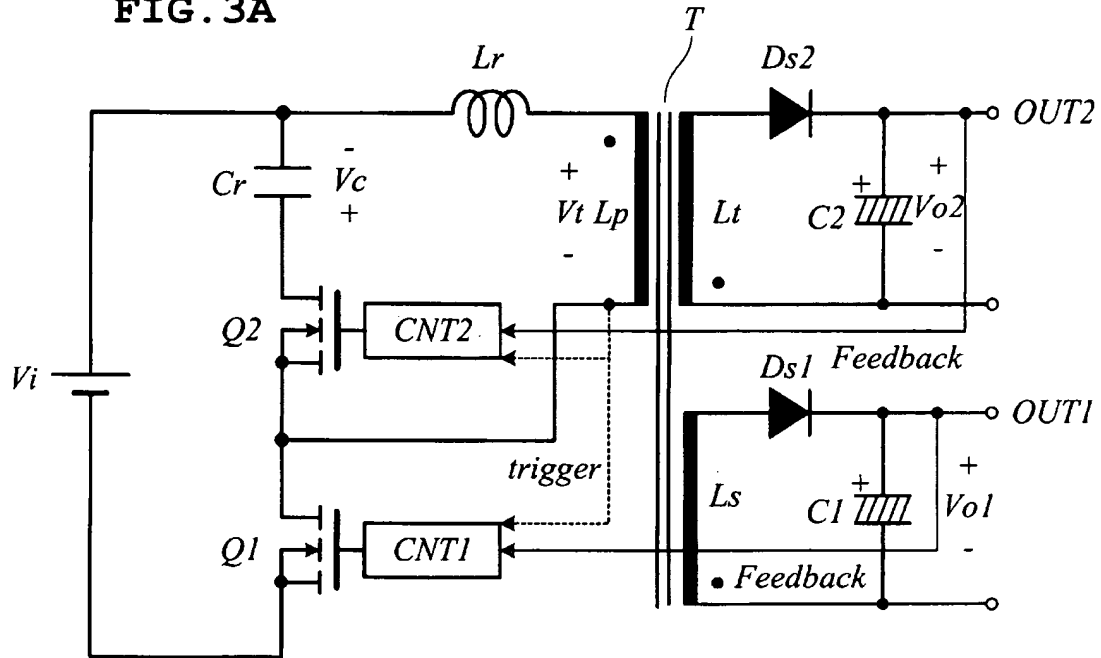


FIG. 3B

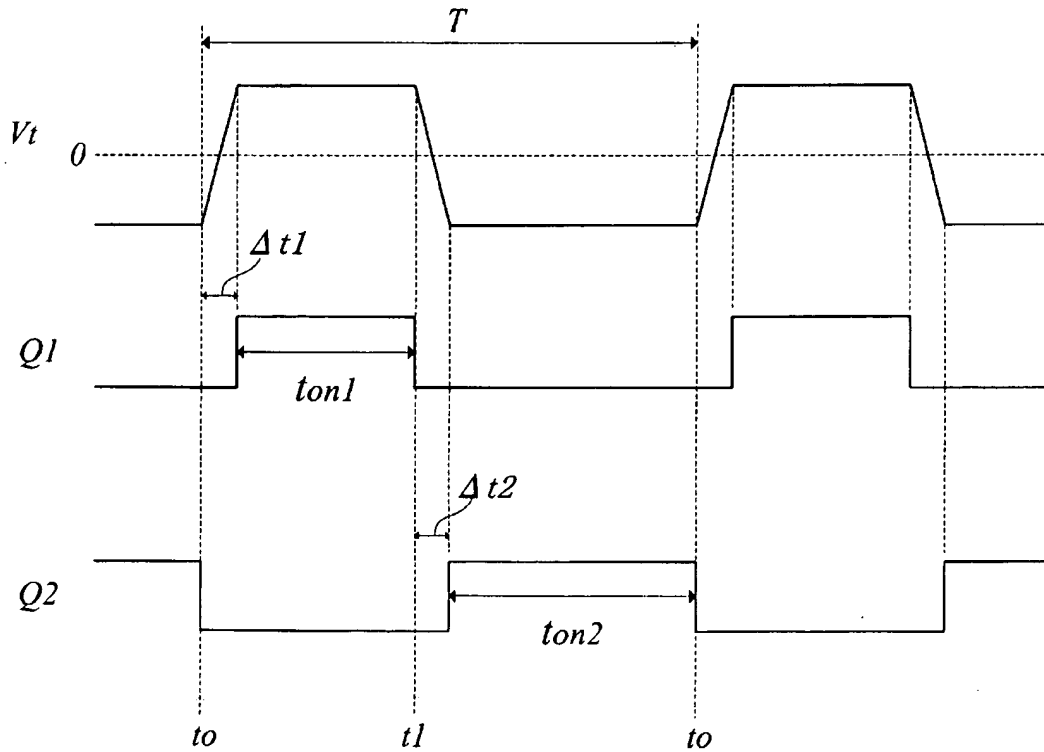


FIG. 4A

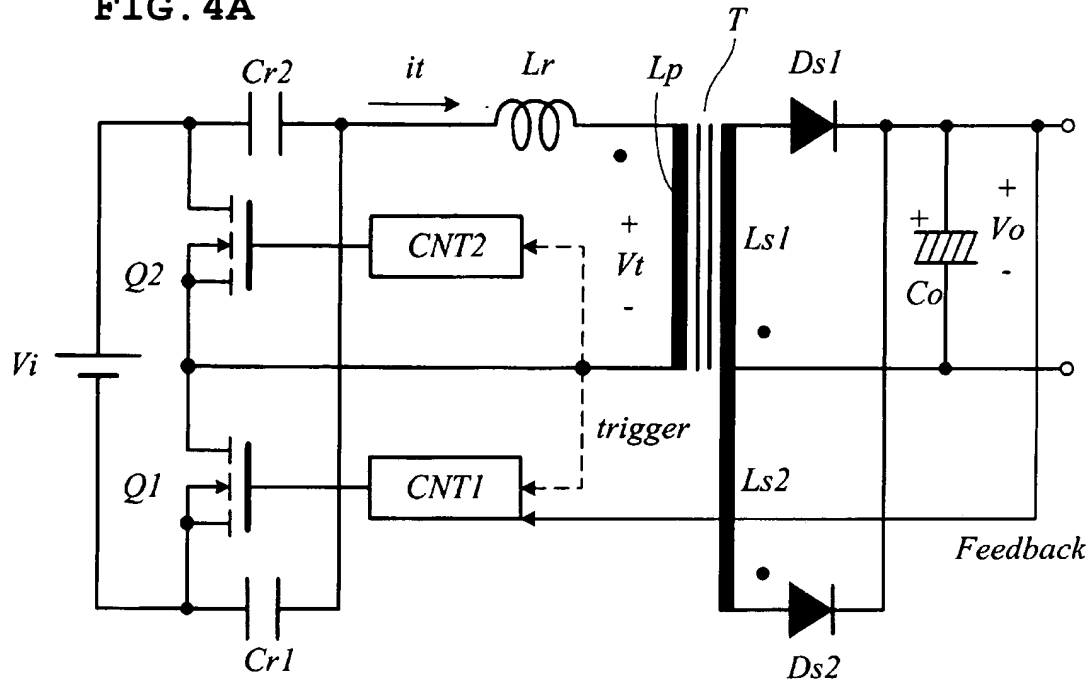
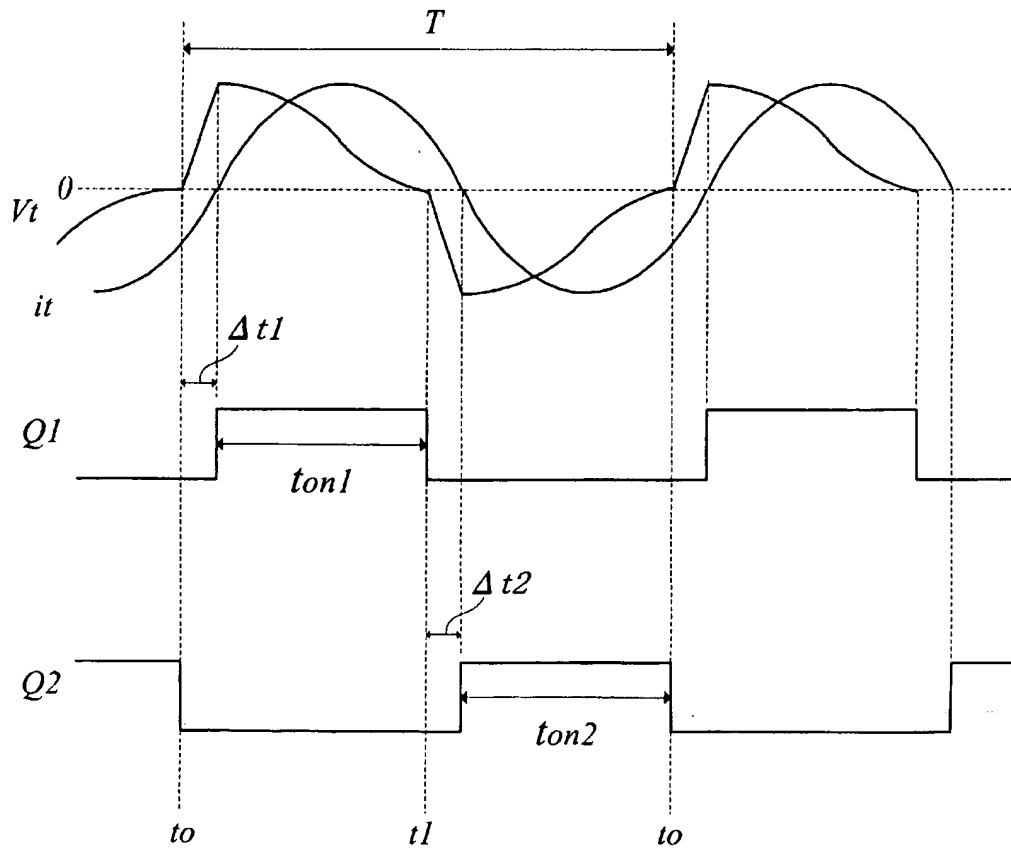


FIG. 4B



**FIG. 5A**

The circuit diagram shows a power converter with a feedback control system. The main power stage consists of an input voltage source  $V_i$  connected to a series combination of a capacitor  $C_r$  and an inductor  $L_r$ . The voltage across  $C_r$  is  $V_c$ . Following  $L_r$ , there is a transformer with primary inductance  $L_p$  and secondary inductance  $L_s$ . The primary voltage is  $V_t$ . The secondary is connected to a diode  $D_s$  in series with an inductor  $L_s$ . The output current is  $i_s$ . The output voltage is  $V_o$  across a load capacitor  $C_o$ . The control system includes two comparators,  $CNT1$  and  $CNT2$ , and two transistors,  $Q1$  and  $Q2$ . The output voltage  $V_o$  is fed back to  $CNT1$  and  $CNT2$ . The output of  $CNT1$  drives  $Q1$ , and the output of  $CNT2$  drives  $Q2$ . The gates of  $Q1$  and  $Q2$  are connected to the primary of the transformer. A 'trigger' signal is also connected to the primary. The transformer is labeled with a dot on the primary and a dot on the secondary.

The diagram shows the timing relationships for a two-phase inverter. The top trace is the gate voltage  $V_t$ , which is a periodic trapezoidal wave with period  $T$ . The middle trace is the source current  $i_s$ , which is zero during the dead time intervals. The bottom traces are the gate signals for the two transistors,  $Q1$  and  $Q2$ .  $Q1$  is high during the first half-cycle and  $Q2$  is high during the second half-cycle. The dead time  $\Delta t$  is the interval between the falling edge of one gate signal and the rising edge of the other. The total dead time for both transistors is  $2\Delta t$ . The time intervals  $t_{on1}$  and  $t_{on2}$  are the conduction times for  $Q1$  and  $Q2$  respectively. The time  $t_0$  is the time from the start of the first half-cycle to the start of the dead time. The time  $t_1$  is the time from the start of the first half-cycle to the end of the dead time. The time  $t_2$  is the time from the start of the first half-cycle to the start of the second half-cycle.